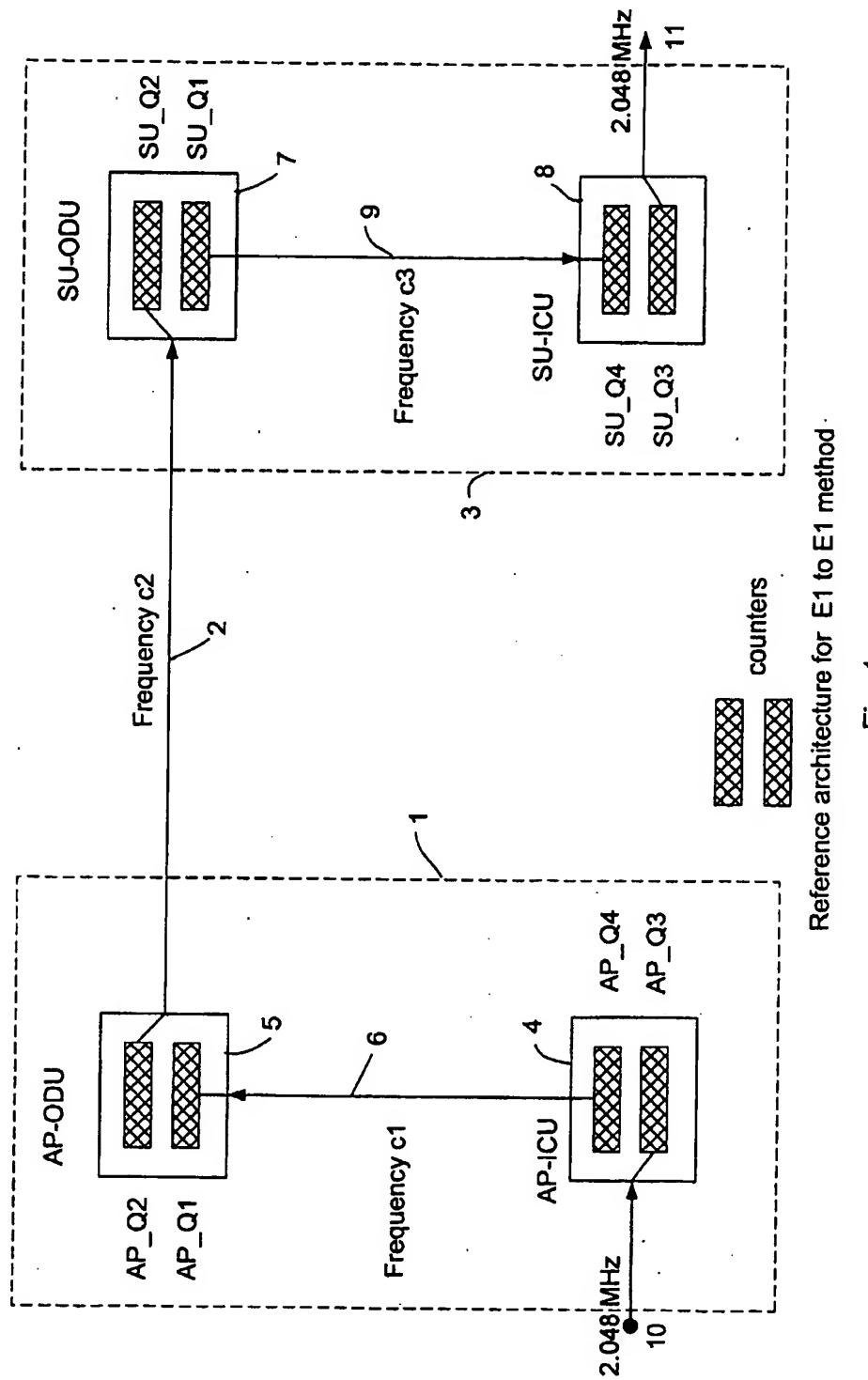


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Reference architecture for E1 to E1 method

Fig. 1

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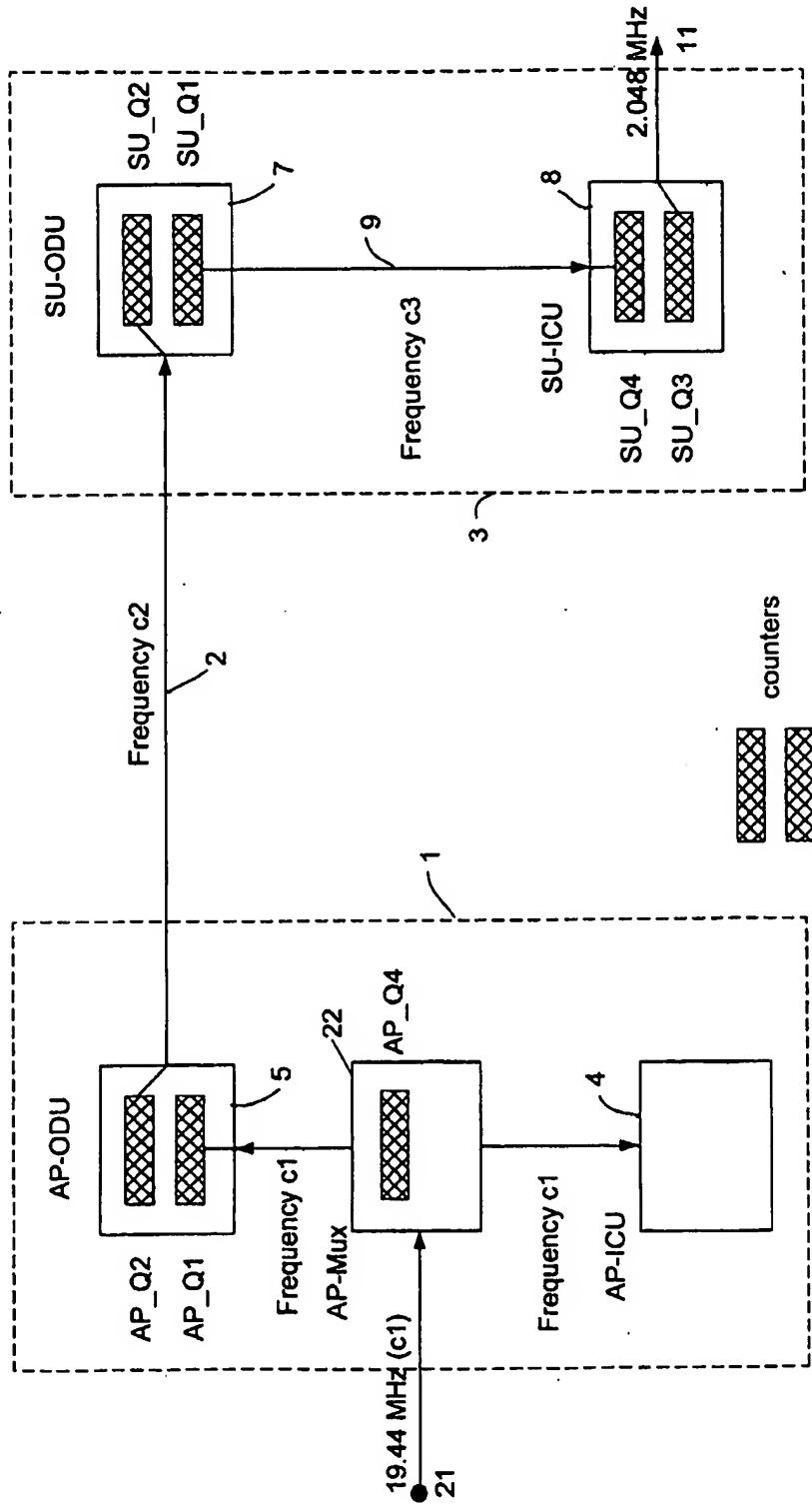
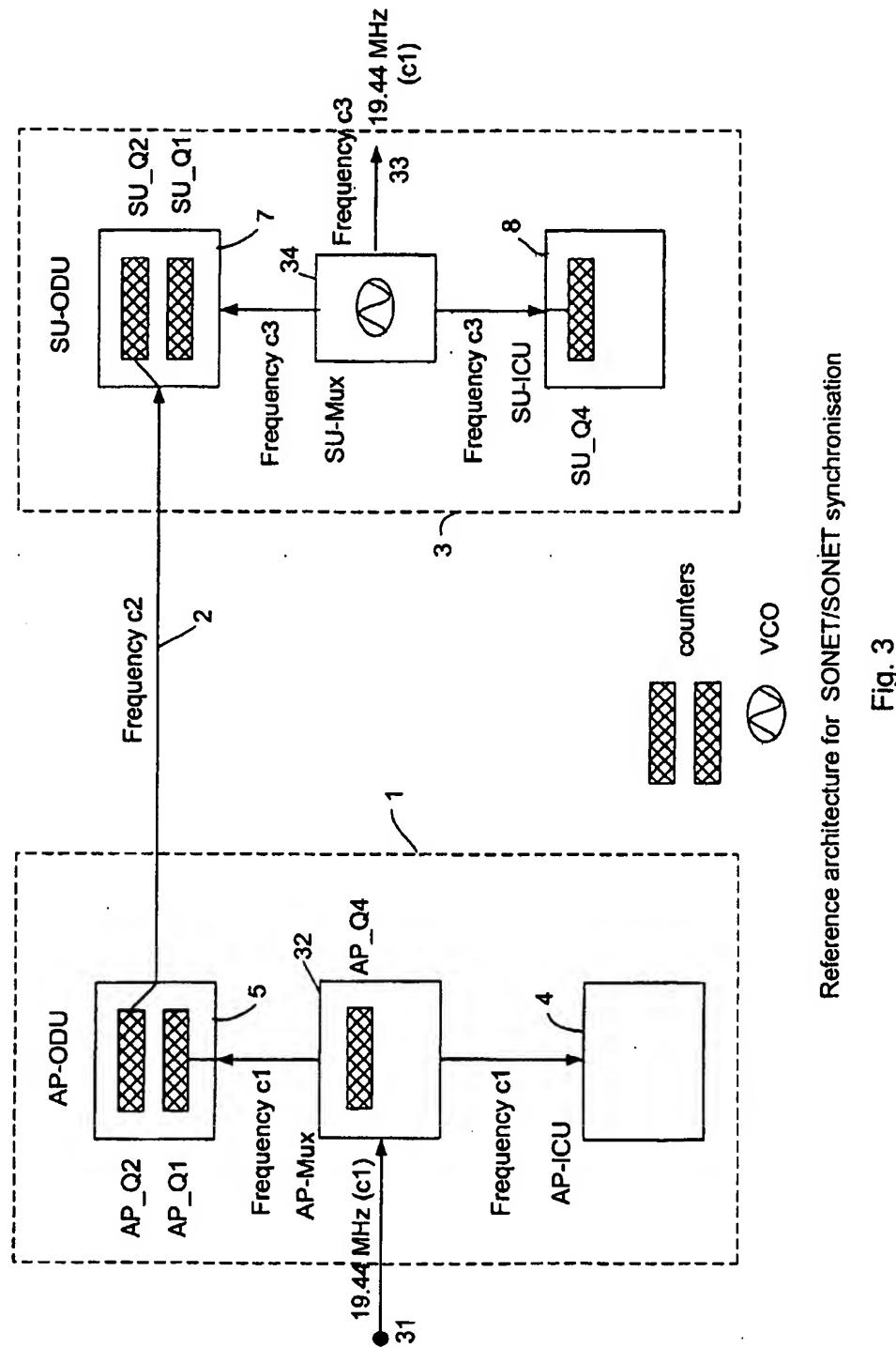


Fig. 2

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Reference architecture for SONET/SONET synchronisation

Fig. 3

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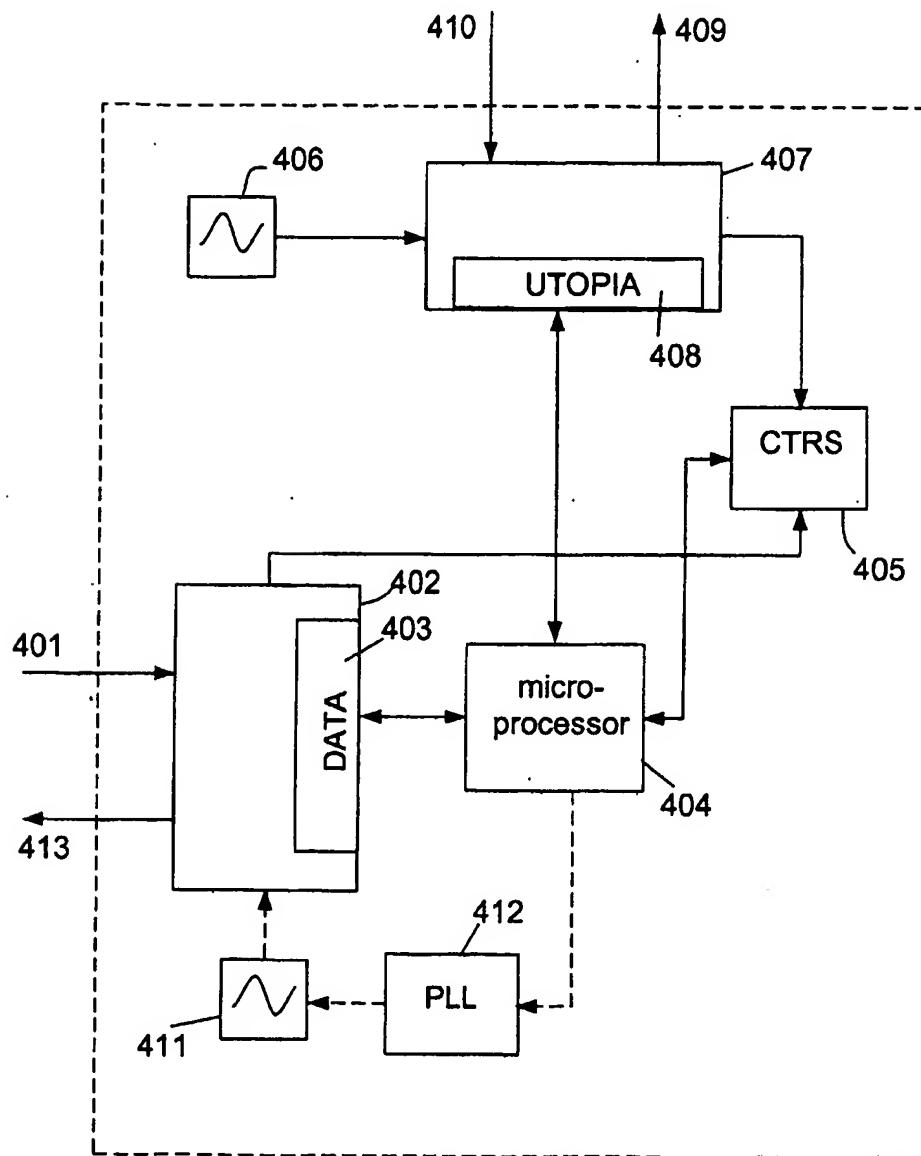


Fig.4

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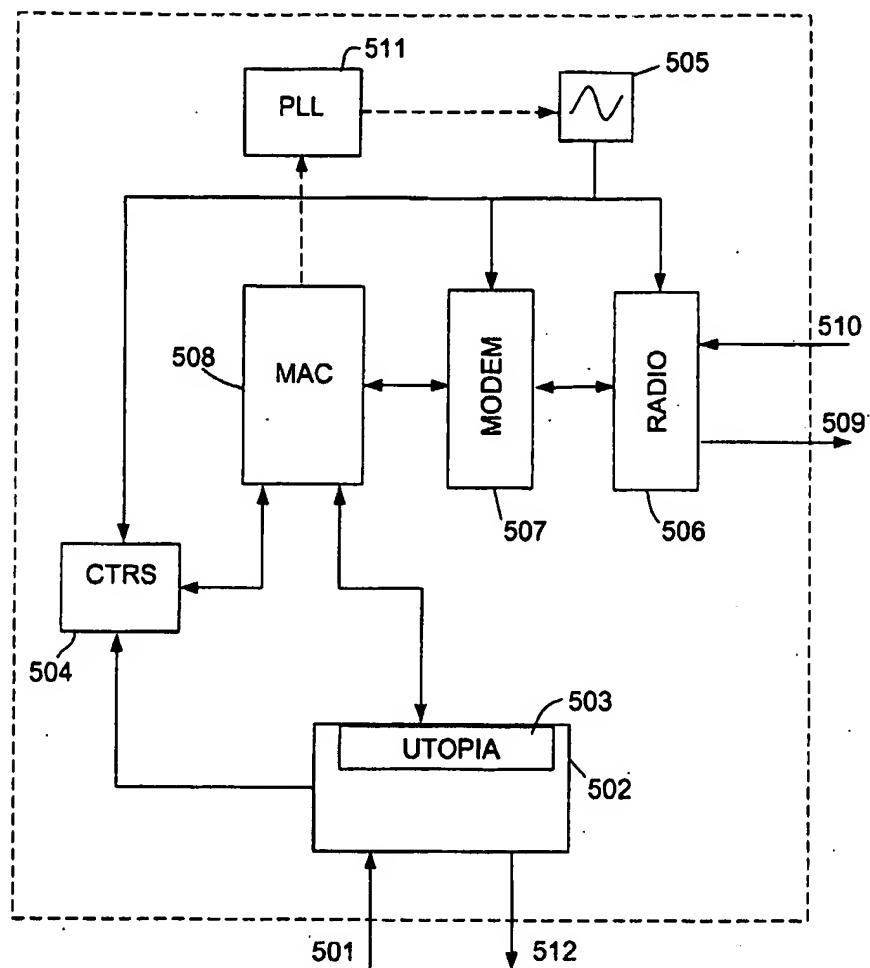
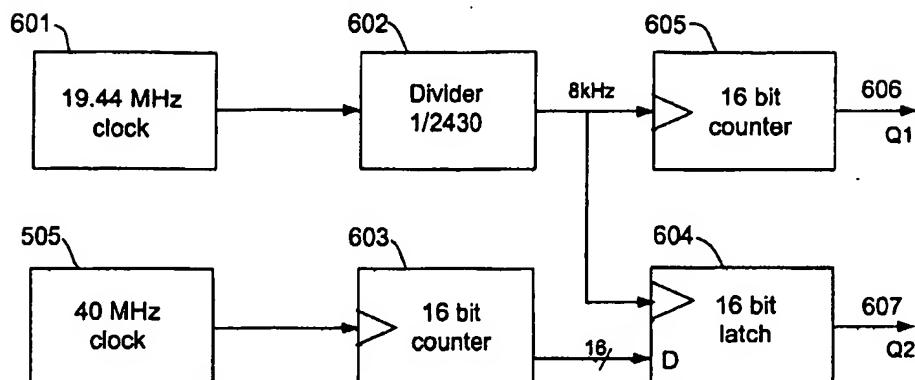


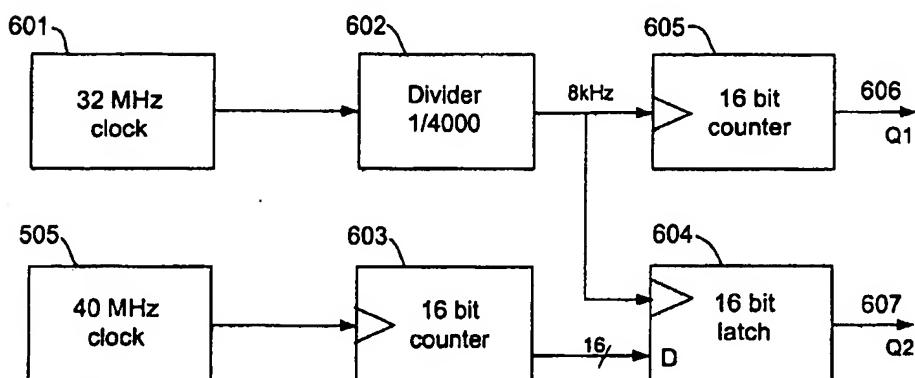
Fig.5

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MAC counter structure for ATM 155 ODU

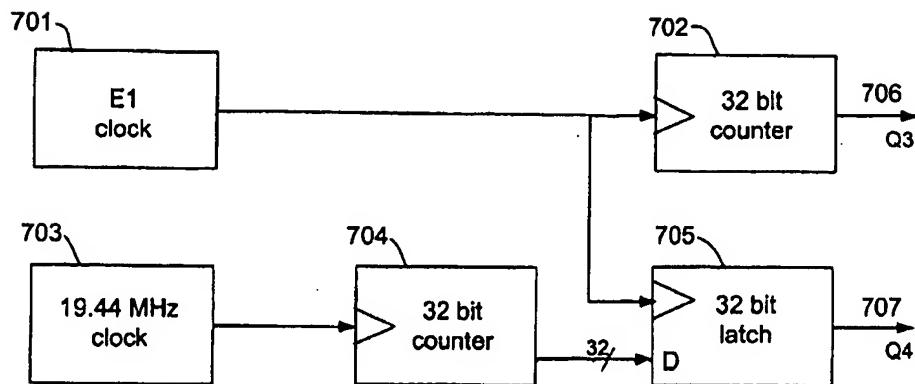
Fig.6



MAC counter structure for ATM 25 ODU

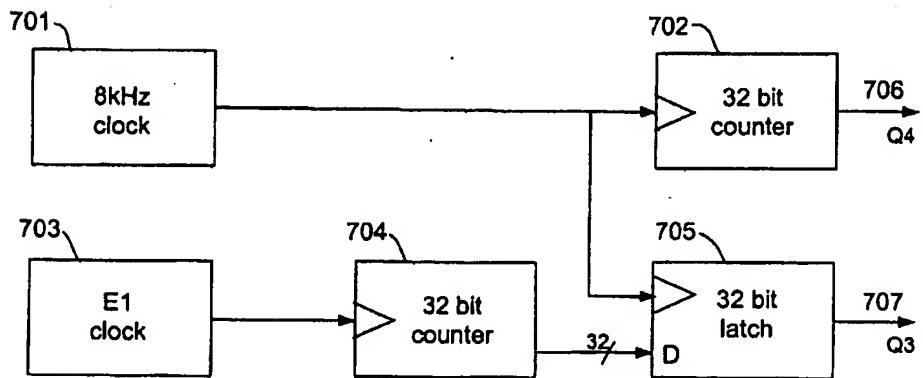
Fig.7

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ATM 155 ICU counter structure

Fig.8



ATM 25 ICU counter structure

Fig.9

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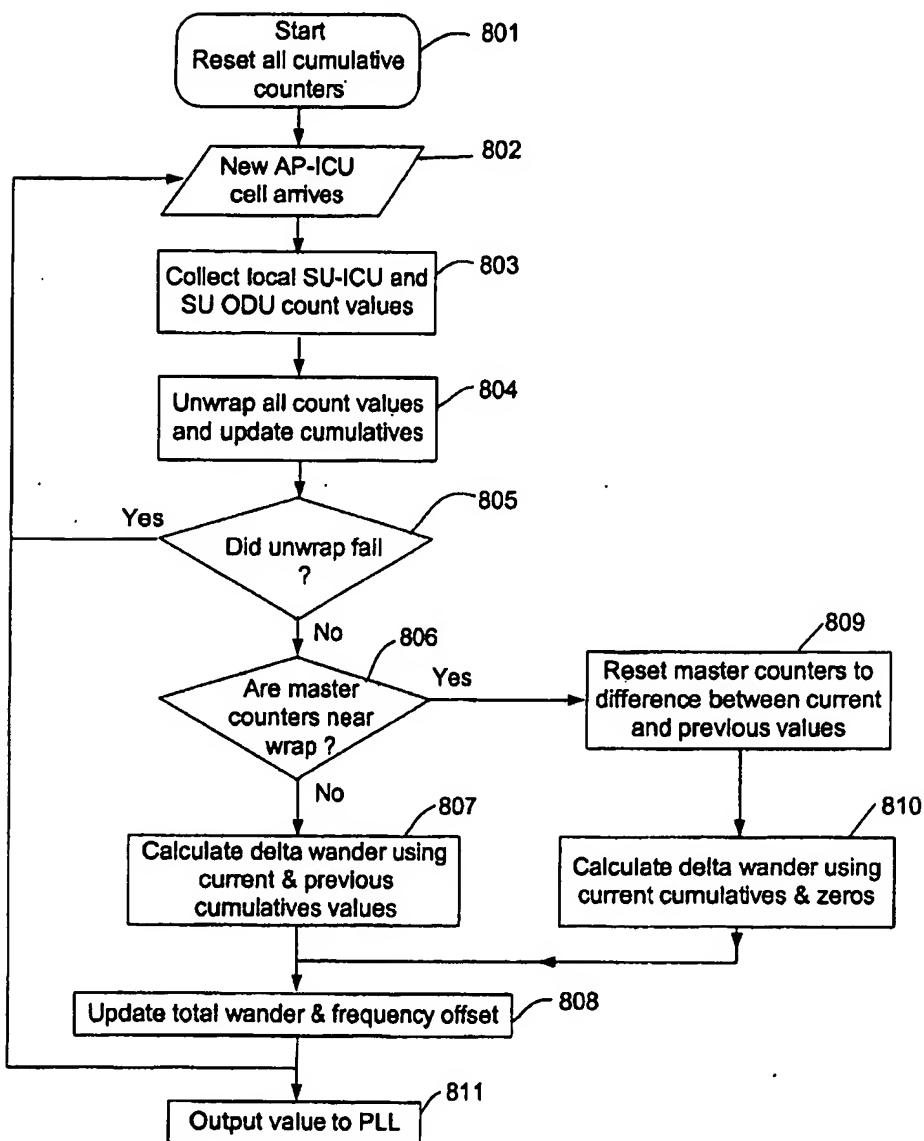


Fig.10

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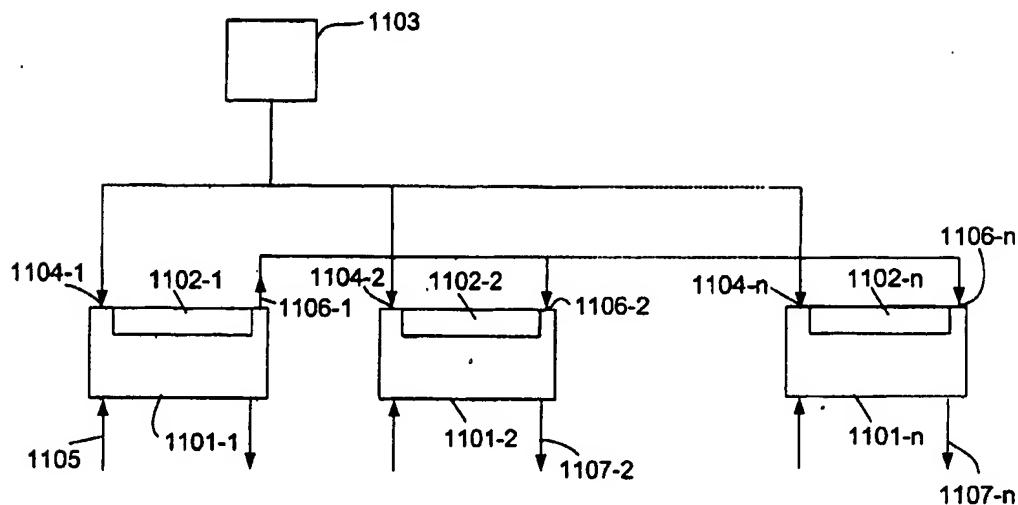


Fig.11

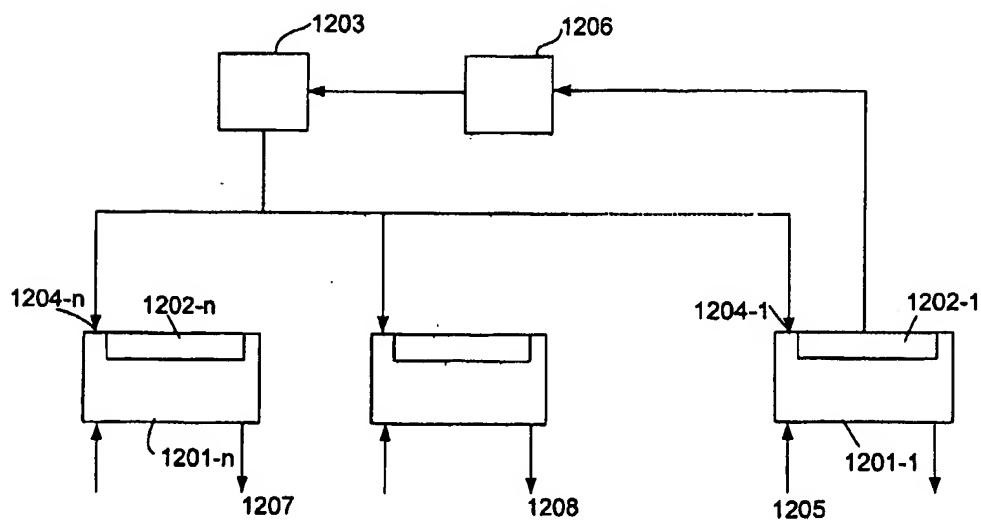
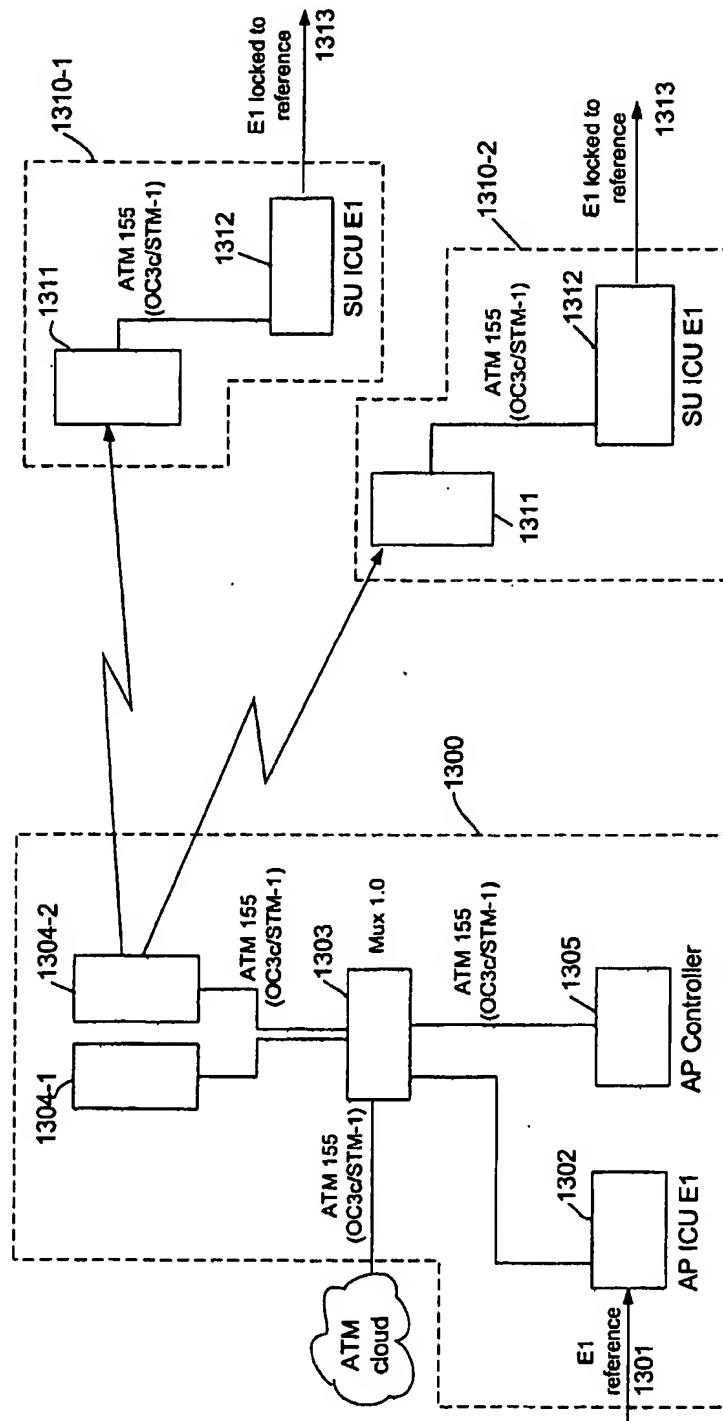


Fig.12

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E1 Synchronisation Architecture 1  
The Reference clock is an E1 at the Base Station. All CPEs on all sectors are phase locked to the reference E1.

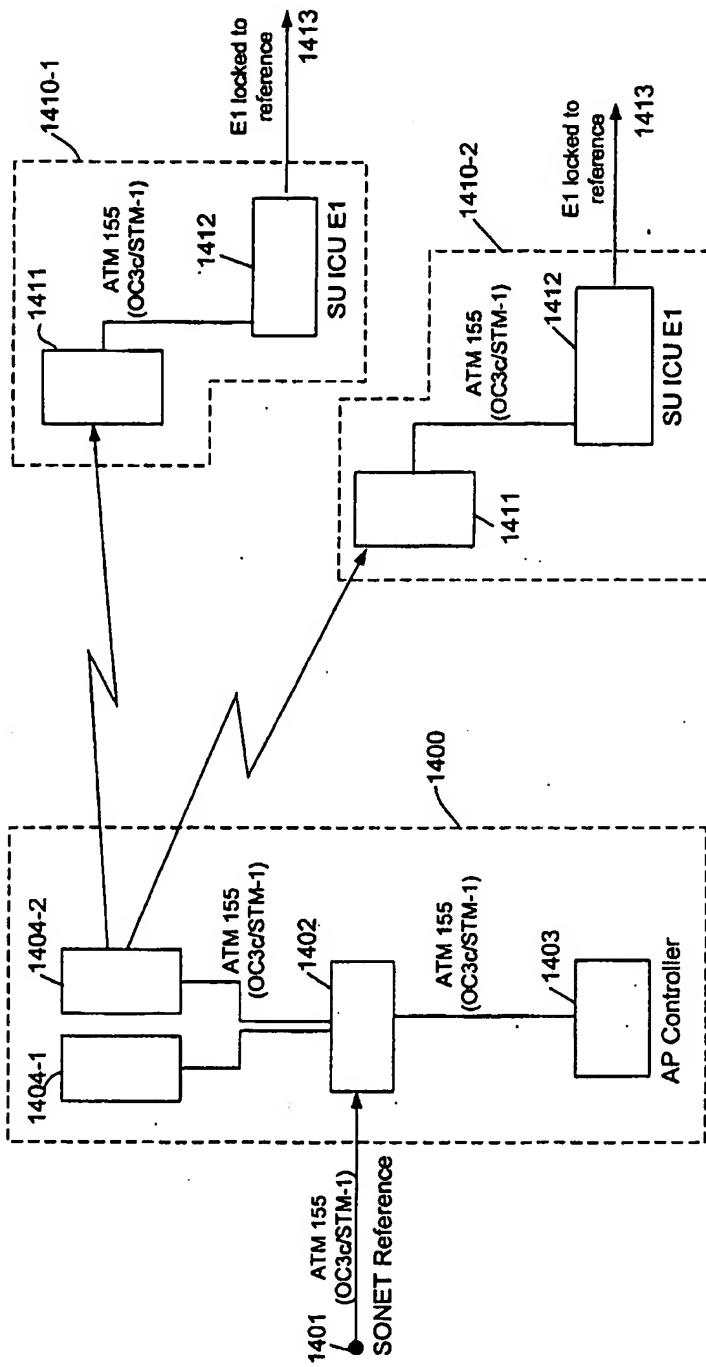


E1 Synchronisation Architecture 1

Fig.13

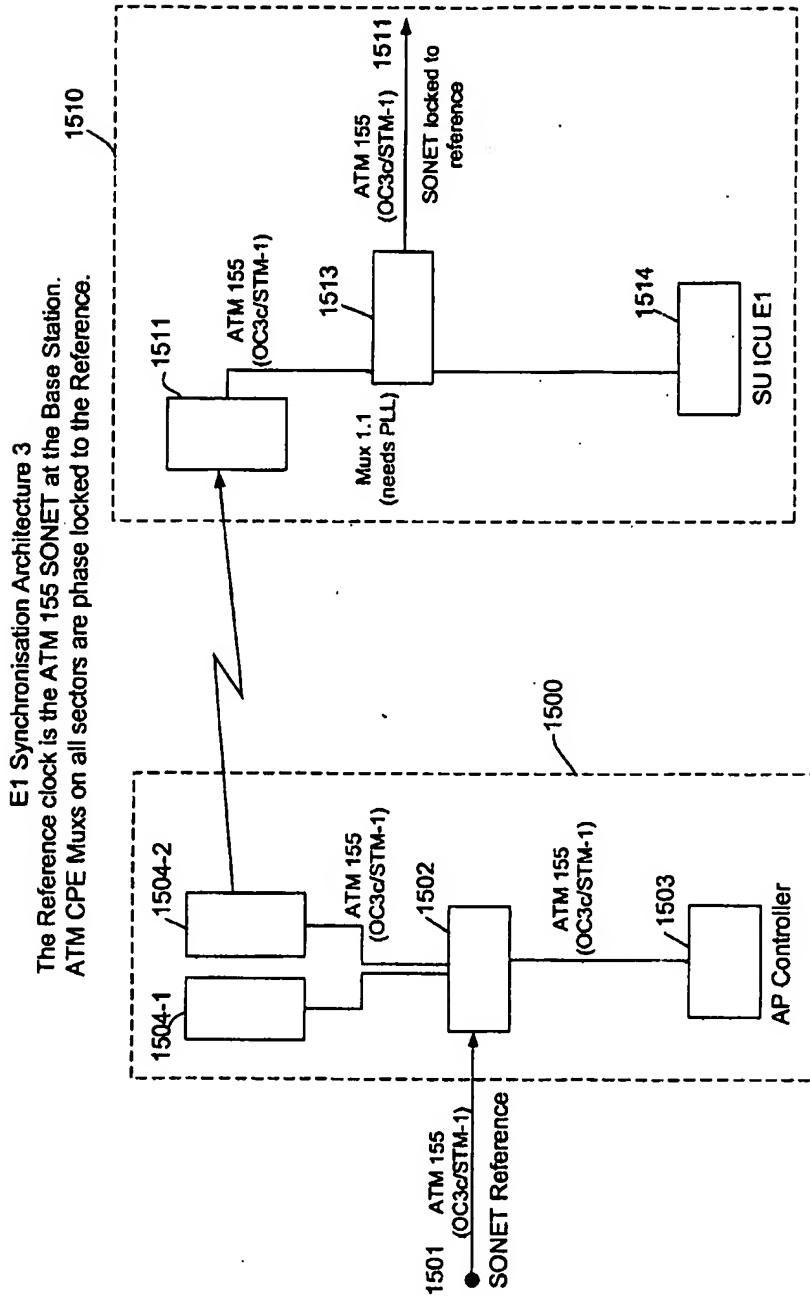
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**E1 Synchronisation Architecture 2**  
**The Reference clock is the ATM 155 SONET at the Base Station. CPEs on all sectors are phase locked to the reference.**



**E1 Synchronisation Architecture 2**  
**Fig.14**

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E1 Synchronisation Architecture 3

Fig.15

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E1 Synchronisation Architecture 4  
The Reference clock is the ATM 155 SONET at one CPE.  
CPEs on that sector ONLY are phase locked to the Reference.

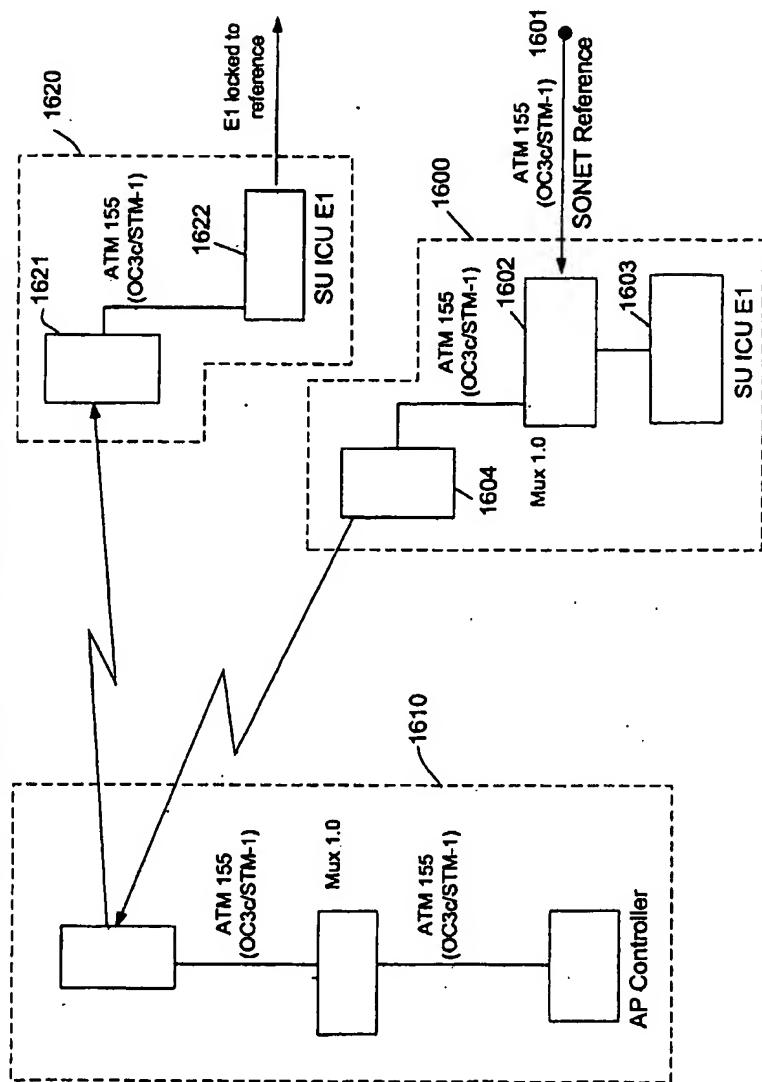
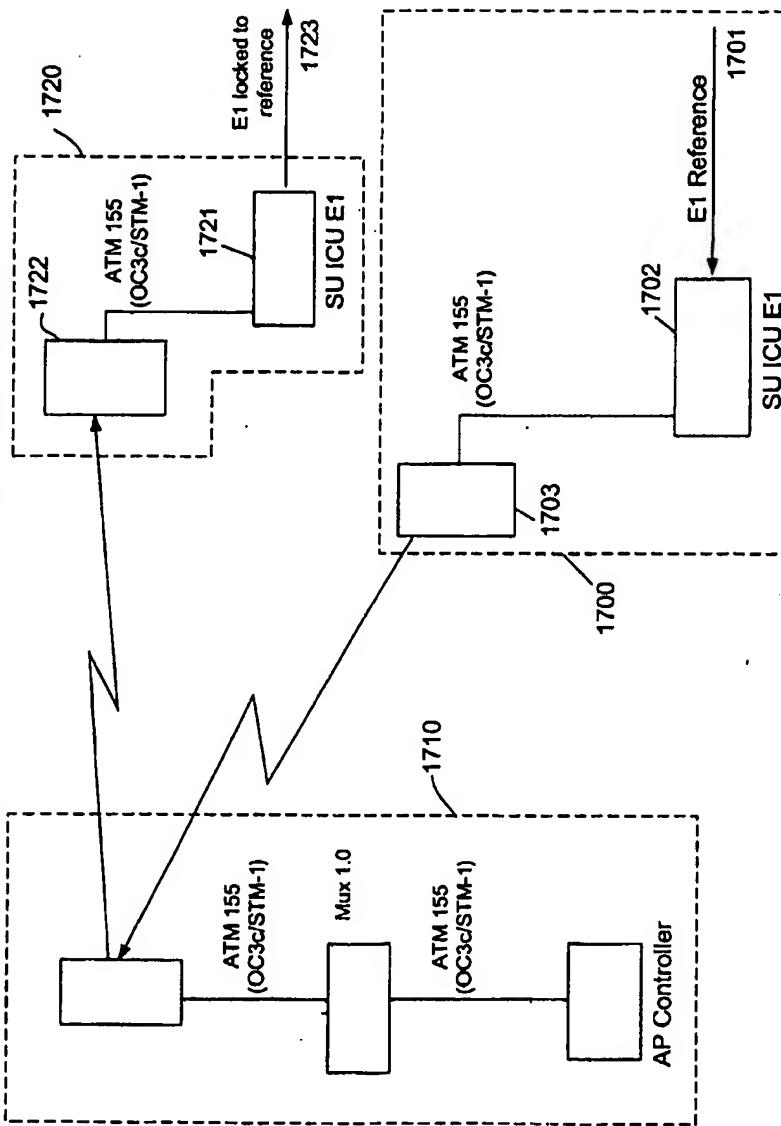


Fig.16 E1 Synchronisation Architecture 4

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**E1 Synchronisation Architecture 5**  
**The Reference clock is one CPE E1.**  
**CPEs on that sector ONLY are phase locked to the Reference.**



**Fig.17 E1 Synchronisation Architecture 5**

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E1 Synchronisation Architecture 6  
The Reference clock is one CPE's ATM 155 SONET.  
ATM CPE Muxs on that sector ONLY are phase locked to the Reference.

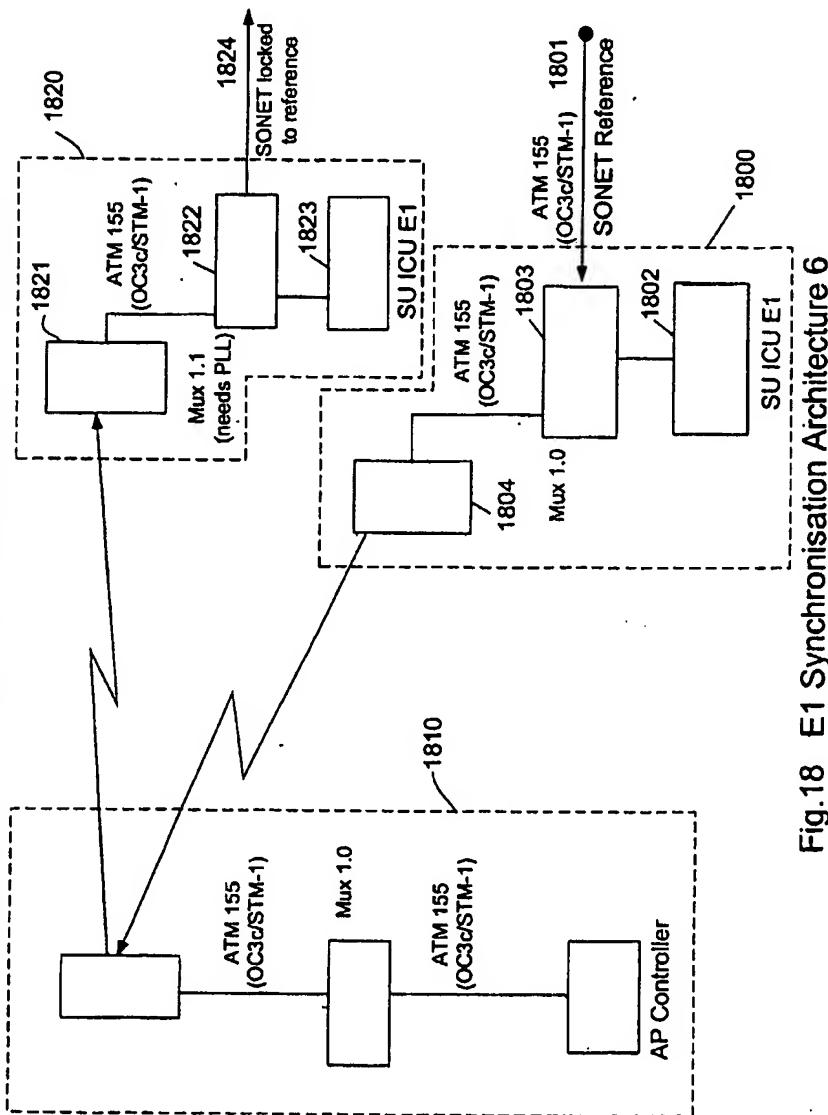


Fig.18 E1 Synchronisation Architecture 6

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**E1 Synchronisation Architecture 7**  
The Reference clock is an E1 at one CPE. All CPEs on all sectors are phase locked to the Reference.

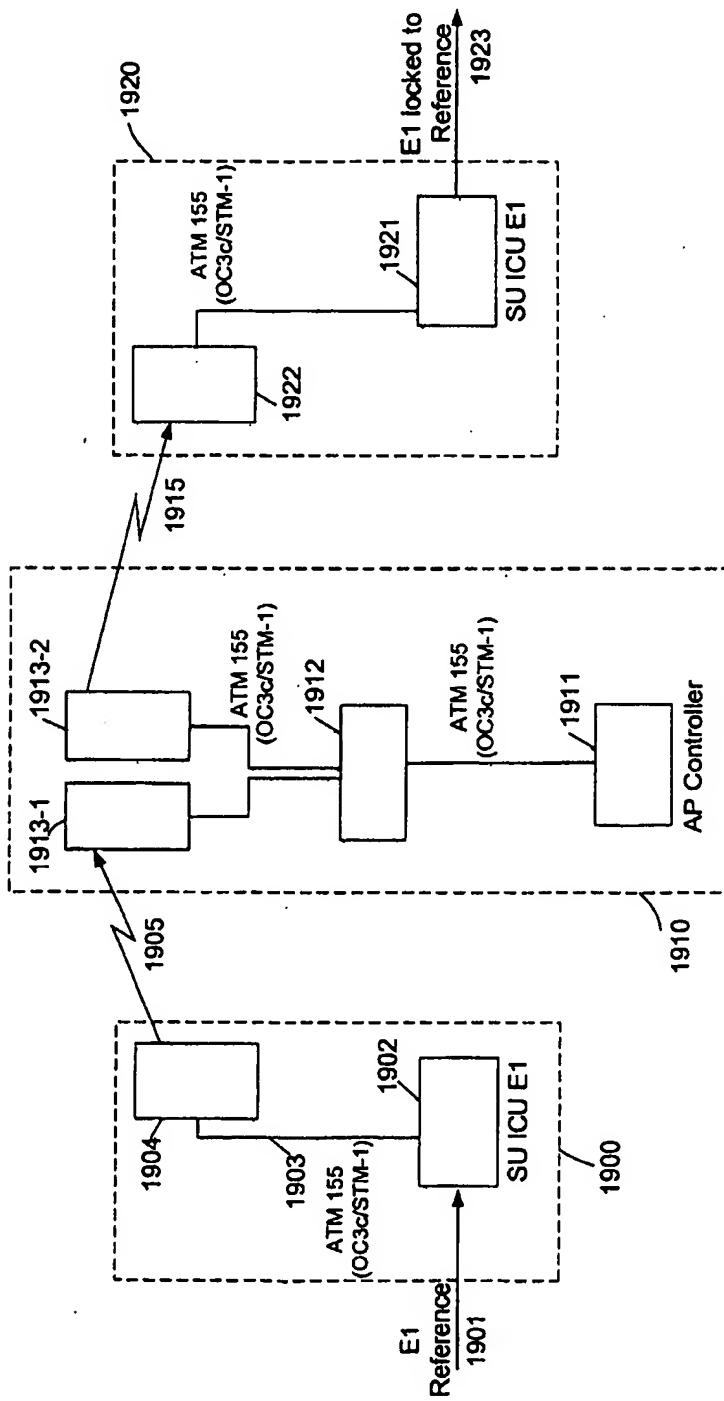


Fig.19 E1 Synchronisation Architecture 7

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E1 Synchronisation Architecture 8  
The Reference clock is SONET at one CPE. All CPEs on all sectors are phase locked to the Reference.

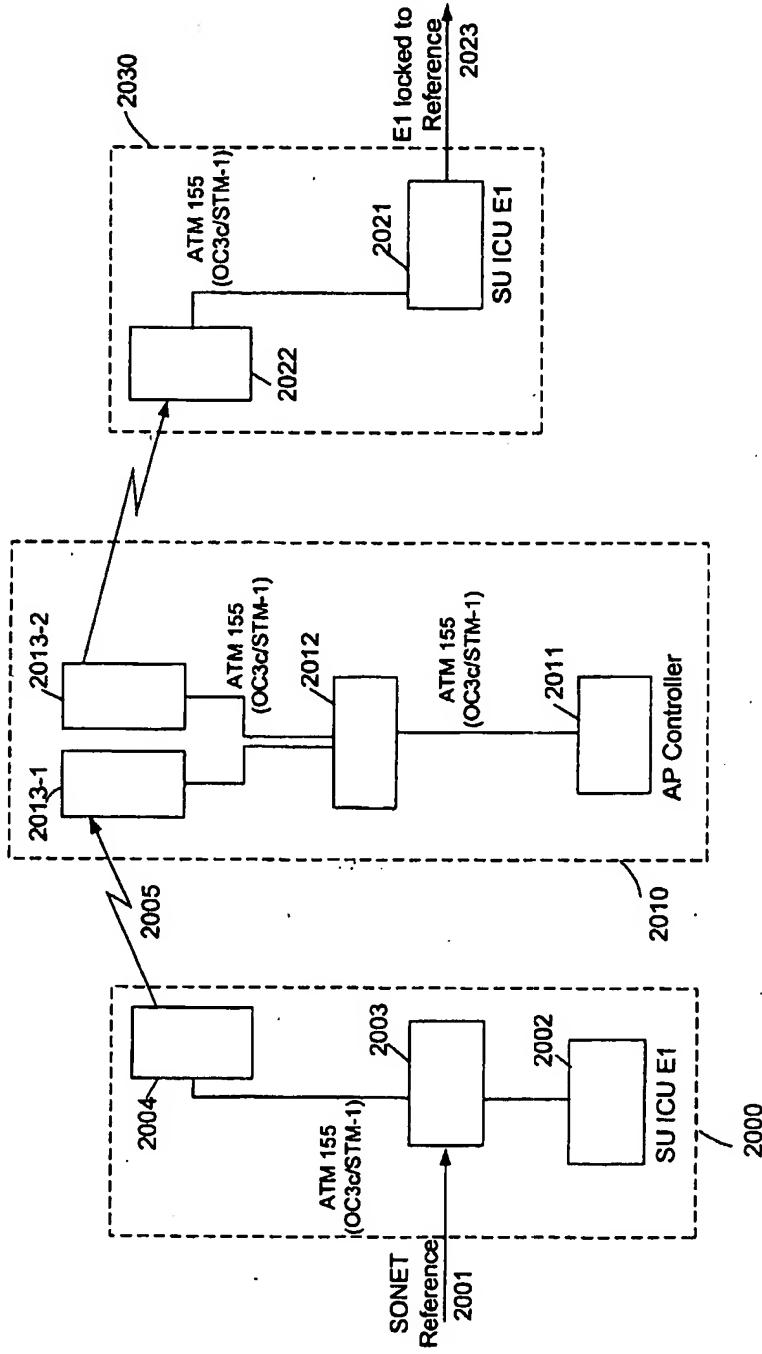


Fig.20 E1 Synchronisation Architecture 8

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**E1 Synchronisation Architecture 9**  
The Reference clock is SONET at one CPE. All SU-Muxs on all sectors are phase locked to the Reference.

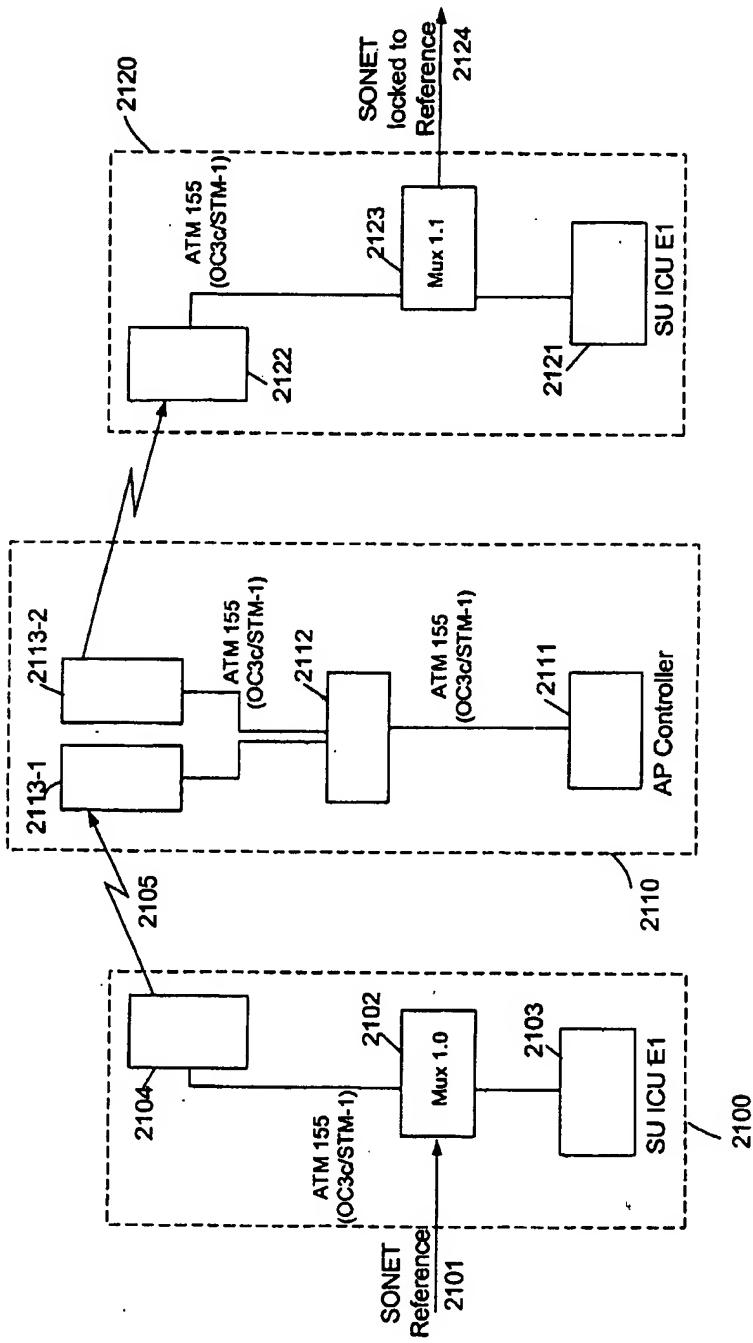


Fig.21 E1 Synchronisation Architecture 9

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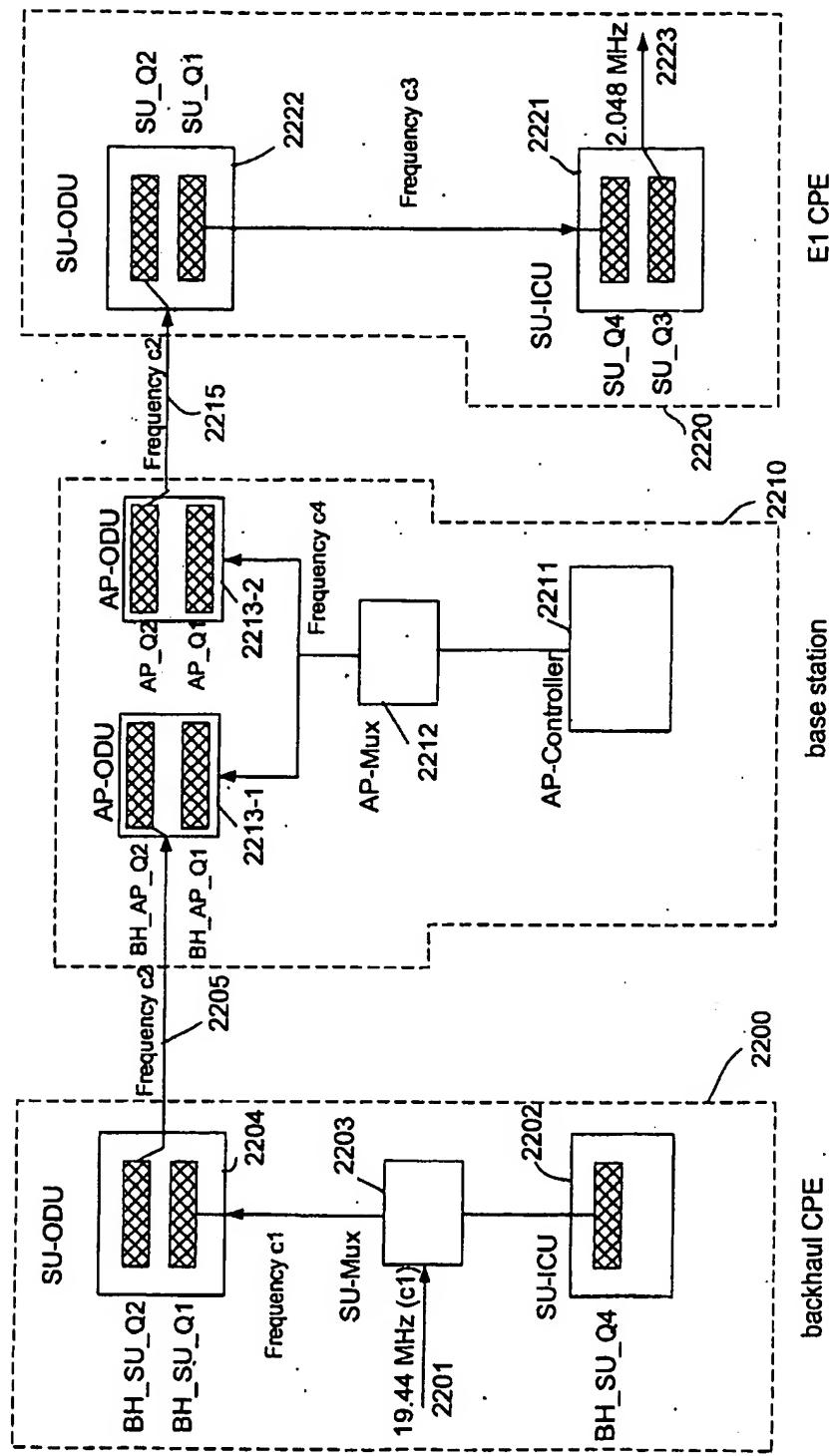


Fig.22 China demo counter architecture

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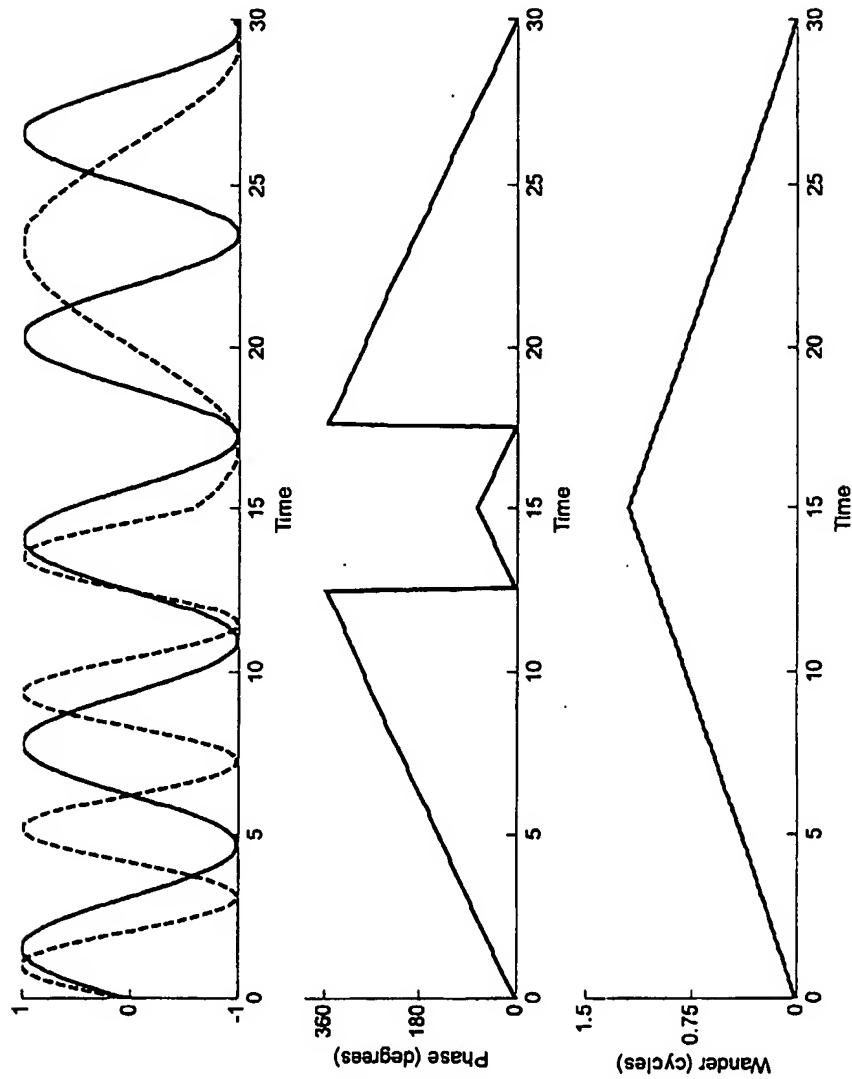


Fig. 23a

Fig. 23b  
Instantaneous Phase  
Difference between  
waveforms

Fig. 23c  
Wander between  
waveforms